Remarks

Claims 1 - 22 are pending in this action. Claims 11 – 22 stand withdrawn and Claims 1 - 10 stand rejected. By this amendment claims 1-8 and 10 have been amended, claim 9 has been canceled, and claims 23 – 36 have been added to place the Application in better position for allowance. Applicants respectfully request reconsideration of all pending claims herein.

Applicants respectfully submit that the amendments to claims 1 - 10 more clearly define and claim Applicants' invention and provides sufficient enablement to meet 35 U.S.C. § 112 paragraphs 1 and 2 requirements and the statutory subject matter requirements of 35 U.S.C. § 101.

Applicants respectfully submit that new claims 23-36 claim the subject matter in the specification related to the use of the circuit model claimed in claims 1-10 (see Applicants' Fig. 6). No new matter has been added to the application by virtue of the present amendment.

In the Drawings

The Office Action stated an objection to Figures 1 - 8 as failing to comply with 37 CFR 1.84 because the copies are too light. A replacement set of drawings is attached hereto in Appendix A of this amendment to overcome the Examiner's objections. Applicants submit that the replacement drawings comply in all respects with 37 CFR 1.84.

In addition, Applicants have amended Fig. 7 element 25 from "circuit module 25" to "code module 25". A replacement sheet for Figure 7 reflecting this change is also attached in Appendix A.

In the Specification

Applicants have amended paragraphs: 31, 38, 46, 79, 87, and 95 to comply with requests for correction outlined in the Office Action pages 2-3.

Regarding the conflict between the terms "circuit module" and "code module" beginning in p80, applicants have amended Figure 7 to include "code module 25" and have ensured that no references to "circuit module" are present in the specification to avoid any confusion. The term "circuit module" in p87 was amended to "circuit model" because the term "circuit module" was used incorrectly in that context.

Claim Rejections – 35 U.S.C. §112, first paragraph

The Office Action states that claims 1 – 10 are rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement. The Office Action stated that claims 1 and 8 are drawn to a tangible circuit device and that there appears to be no support in the application as filed for a tangible circuit device.

Applicants have amended claims 1-10, to replace the references to a tangible circuit device, with references to a circuit model of a black box circuit and the method of simulating a black box circuit. The circuit model is shown in Applicant's figures 1-5. Specifically, the circuit model incorporates the functionality of resistors, capacitors, current, and voltage drivers, and is used to model a black box circuit design, thus the circuit model of the present invention is used during simulation so that the details of the real circuit design remain hidden to the user (See Lehner Figure 1 ckt A, para. 22). The black box circuit is a representation of a proprietary or otherwise confidential circuit (i.e. intellectual property), which is provided to a customer who endeavors to use the circuit either alone or in a larger IC design. Thus, Applicants' claimed invention provides a means for the IP owner to maintain the propriety of the circuit design while enabling the customer to use the design.

The Office Action stated that claims 1, 4, and 6 recite limitations wherein a function is defined in terms of other functions, "collectively"; but there appears to be no support in the specification to support the limitations. The Office Action requested the citations of specific portions of the disclosure which support the above stated limitations.

Applicants have amended claims 1, 4 and 6 to remove the term "collectively", because it is redundant in view of the recitation of required functions already listed in each respective claim.

The Office Action stated that claims 1-3 and 5-7 recite several limitations which provide circular and conflicting descriptions of the first and second current functions of the invention; and that there does not appear to be support in the specification for any of these claims. The Office Action requested the citations of specific portions of the application which support the limitations stated above.

Applicants respectfully submit that the most exemplary support for the limitations in claims 1-3 is shown in Figure 2 of Applicants' specification. Figure 2 shows: an output node – Vout, a first and second current function – Ip and In respectively, a first voltage function – Vin, A first, second, and third capacitance function – Cin, Cm, and Cout, and an internal impedance function – Zint. The first and second current functions are further explained in paragraph 23 of Applicants' specification as "full functions of all input voltages (Vin) and all output voltages (Vout)" (See Lehner Claim 2).

Claim 5 further limits the first and second current functions of claim 1 as functions of a p-block behavioral model and an n-block behavioral model respectively. The p-block and n-block behavioral models are defined in Applicants' specification paragraph 2 and Figure 4 and are simplified representations of CMOS circuitry that are commonly known to those skilled in the art.

Claims 6 and 7 depend from claim 5. Claim 6 further limits the simplistic p-block behavioral model to function as a result of all of the input node values and all of the output node

values of the circuit model (See Lehner para. 23). Claim 7 further limits the first and second current sources of claim 5 to each be dependant on a portion of input and output node values rather than all possible input and output node values (See Lehner para. 35 and 65).

Applicants have in amended claims 1- 8, and 10, canceled claim 9, and cited specific references to descriptions in Applicants' specification to overcome the rejection for failing to comply with the written description requirement. Applicants therefore submit that the 35 U.S.C. §112 first paragraph rejection of claims 1-10 has been overcome.

Claim Rejections – 35 U.S.C. §112, second paragraph

The Office Action stated that claims 1-10 stand rejected under 35 U.S.C. §112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Office Action stated that "because the claim language is so different from the specification, it is impossible to ascertain what is meant by these conflicts or whether the claims are improper dependent claims. The disconnect between the claim terminology and the specification and the several indefinite claims make it difficult to determine which of the recited limitations are indefinite and which are clear in light of the specification".

The Office Action stated that claim 1 was previously rejected for"

> *[...] reciting "a circuit" defined in terms of intangible components, and therefore not "a circuit". Claim 1 was amended to recite "an integrated circuit device comprising elements, wherein the elements comprise characteristics and parameters in accordance with a circuit model, wherein the circuit model comprises [several limitations]." Therefore, claim 1 is vague and indefinite. In summary, the Office Action stated that it was unclear whether claim 1 is directed to a tangible circuit with resistors, capacitors, etc. or to an abstract circuit model which represents a tangible circuit. The Office Action further stated that limitations such as "a first and second current function", "a first voltage function", and "a first, second, and third impedance function", etc. encompass enormous breadth and fail to distinguish the invention from prior art.*

Applicants have amended claim 1 to distinctly claim the circuit model of a black box circuit as the model exists in a memory device. Applicants further submit that the current, voltage, and impedance functions of claim 1 are mathematical functions used as inputs, outputs, and loads which supply the values necessary to model the response of the real circuit under specified conditions in such a way that the details of the real circuit remain hidden from the user.

The Office Action stated that the rejection and analysis applied to claim 1 also applies to claim 8 and that "[T]he Examiner is aware of no such object as "an impedance" which can be "connected to the output node and ground." To the best of the Examiner's knowledge, impedance is a property, not an object or element with connections".

Applicants have amended claim 8 to recite "[…] an internal impedance *value* between the output node and ground." to clarify that impedance value between an output node and ground is required to simulate the black box circuit (see Lehner para 24 and 46, fig. 2 and 5).

The Office Action stated that:

> *Applicants' response (page 9) states that "Applicants have amended independent Claims 1 and 8 to be directed toward a physical IC device, which has elements, which in turn have characteristics and parameters in accordance with a circuit model." This statement in the record appears to substantiate the Examiner's interpretation of claims 1 and 8 and further necessitates this rejection under 35 U.S.C. § 112, second paragraph.*

As stated above, Applicants have amended claims 1 and 8 to be directed to a circuit model contained in a memory device; not to a physical IC device.

The Office Action stated that:

> *Claims 1, 4, and 6 recite claim language including a "function" that is a "function of [several limitations], collectively." It is unknown if this claim language is an attempt at defining a conjunctive or disjunctive*

> *list of limitations. It is unknown if every recited element in the list is required to define the recited "function". In general, it is unknown what that term "collectively" means in the context of defining a function.*

As stated above, Applicants have amended claims 1, 4, and 6 to remove the term "collectively" because it is explicit in each of the respective claims that the output node value is a function of the several other functions listed. Furthermore, the concept of a function defined in terms of multiple other functions is well known to those of ordinary skill in the art of computer programming (see Lehner para 27, 34, 29-30, 42-43, and 64).

The Office Action stated that:

> *Claim 4 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is unknown what is meant by "a near capacitor function," "a resistor function," or "a far capacitor function." The Examiner has reviewed the specification and cannot identify where support for this terminology exists.*

Applicants respectfully submit that support for "a near capacitor function", is listed in Applicants' specification paragraphs 86-87, 94, and 100 and is represented by the nomenclature "Cnear_o". Support for "a resistor function" is located in Applicants' specification paragraphs 25, 29-31, 51-52, 59, and 79, and figure 3; and is represented in some instances by the nomenclature Rg, Rload, and R. Support for "a far capacitor function" is located in Applicants' specification paragraphs 86-87, 94, and 100; and is represented by the function "Cfar_o".

In regards to claim 5 the Office Action stated that:

> *Claim 5 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.*
>
> *Claim 5 depends upon claims 3, 2, and 1. Claim 5, when written as an independent claim, incorporates all the limitations of the claims from which it depends. See 37 CFR 1.75. Claim 5, when written in*

independent form, contains inter alia the following limitations:

"wherein the output node has a value that is a function of the first and second current function (claim 1)

"wherein the first and second current functions are subsequently functions of the input node voltage value and the output node voltage value" (claim 2)

"wherein the first current function is a function of a p-block behavioral model, and the second current function is a function of an n-block behavioral model" (claim 5)

In addition to presenting what appears to be a circular definition for the first and second current function (the first and second current function are functions of the output node voltage; the output node has a value that is a function of the first and second function), the language of claim 5 appears to define "a p-block (or n-block) behavioral model" as a narrower recitation of "the input node voltage and output node voltage." Barring this interpretation, claim 5 is an improper multiple dependent claims for failing to further limit a parent claim, regardless, the precise meaning of claim 5 is unknown for the reasons set forth above and the claim is therefore vague and indefinite.

Applicants respectfully submit that claim 5 depends *only* from claim 1 (not claims 1-3 as stated by the Examiner) and that the "p-block" and "n-block" behavioral models shown in figure 4 of Applicants' specification are further limitations of the current functions shown in Applicants' figure 2 (Ip and In) as claimed in claim 1. Specifically, the first current function, Ip, is a function of a "p-block" behavioral model, and the second current function, In, is a function of an "n-block" behavioral model (see Lehner para. 59 and 65).

In regards to claim 6 the Office Action stated:

Claim 6 exacerbates the indefiniteness of claim 5, from which it depends. Claim 6 appears to reinstate a portion of the limitations of claim 2 by reciting, "wherein the first current function is a function of each of the input and output node values, collectively." It is at least unclear how this limitation defines the first current function

> *differently from claim 2, and appears to be an improper dependent claim in light of the limitations of claim 5.*
>
> *Claim 6 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 6 appears to contain grammatical errors that render the meaning of the claim unclear. Specifically, claim 6 does not contain a verb in the independent clause. It is therefore impossible to determine what Applicants' intended limitation might be and therefore will not be treated on the merits.*

Applicants respectfully submit that because the rejection to claim 5 has been overcome (see above) that the rejection to claim 6, based on its dependence to claim 5 and the foregoing amendment, has also been overcome. Additionally, the verb in the independent clause recited in claim 6 is the verb "is", i.e. "[…] the first current function *is* a function of each of the input and output node values […]"

In regards to claim 7 the Office Action stated that:

> *Claim 7 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 7 suffers deficiencies similar to claims 5 and 6. The limitations of claim 7 do not further limit the invention as defined by claim 5. It is unclear how to interpret claim 7 when considered in independent form. Does claim 7 define "a function of a p-block behavioral model" as synonymous with "configured to be functionally dependent on a first plurality of input node voltage values and a second plurality of output node voltage values?" Similar problems exist regarding "a second current function" as recited by claim 7.*

Applicants respectfully submit that claim 7 has been amended to further limit the set of input and output values assigned to each p-current source and n-current source. As recited in claim 7, the n-block and p-block current sources may be multiplied and arranged in parallel to form any

number of parallel current sources, each having dependence on a smaller subset of input voltages and output voltage values – rather than the entire set of input and output voltages collectively (see Lehner para.65).

The Office Action concluded that claims rejected but not specifically mentioned stand rejected by virtue of their dependence.

Based on the foregoing arguments, clarifications, and amendments, Applicants submit that the rejection to claims 1-8 under 35 U.S.C. § 112, second paragraph, has been overcome and therefore, the rejection of claim 10 is overcome by virtue of its dependence upon claims 1-8. Claim 9 has been canceled.

Claim Rejections - 35 U.S.C. § 101

The Office Action stated that:

> *Independent claims 1 and 8 are interpreted as being directed to a "circuit model" in order to resolve several rejections under 35 U.S.C. § 112 as set forth above. These interpretations are in keeping with what Applicants have invented, as best understood by the Examiner. (See, for example, specification, paragraphs 0014, 0027). However, a circuit model is non-statutory because it is not a specific machine or apparatus, but is instead an abstract, intangible description of a real circuit's behavior. As such, a circuit model itself is nonfunctional descriptive material. Please see MPEP 2106 (IV)(B)(1).*

Applicants respectfully traverse the Examiner's rejection of claims 1 and 8 under 35 U.S.C. § 101 because claims 1 and 8 have been amended to recite "A memory for access by a circuit simulation program comprising a circuit model [...] stored in the memory [...]" (see Lehner para. 108-109, Fig. 8). Thus claims 1 and 8 and amended are directed to

functional descriptive material.

MPEP 2106 (IV)(B)(1) states in part that:

> *[...] Descriptive material can be characterized as either "functional descriptive material" or "nonfunctional descriptive material." In this context, "functional descriptive material" consists of data structures and computer programs which impart functionality when employed as a computer component. (The definition of "data structure" is "a physical or logical relationship among data elements, designed to support specific data manipulation functions." [...]*
>
> *[...]When functional descriptive material is recorded on some computer-readable medium it becomes structurally and functionally interrelated to the medium and will be statutory in most cases since use of technology permits the function of the descriptive material to be realized. [...][See] In re Lowry, 32 F.3d 1579, 1583-84, 32 USPQ2d 1031, 1035 (Fed. Cir. 1994) (claim to data structure stored on a computer readable medium that increases computer efficiency held statutory) [...]*

In the opinion for *In re Lowry*, the United States Federal Court of Appeals stated:

> *The Board found that claims 1 through 5, directed to a memory containing stored information, as a whole, recited an article of manufacture. The Board concluded that the invention claimed in claims1 through 5 was statutory subject matter.*

Representative Claim 1of the Lowry patent application is shown in part below:

> *A memory for storing data for access by an application program being executed on a data processing system, comprising:*
> *a data structure stored in said memory, [...]*

Because Applicants' claimed invention is directed to a circuit model which is stored in a

memory for access by a simulator application program, the key facts regarding the subject matter of *In re Lowry* are analogous to the facts present in Applicants' Amendment. Thus *In re Lowry* is on point and the opinion handed down by the US Court of Appeals confirming that a data structure stored in a memory *is* statutory subject matter under the meaning of 35 U.S.C. §101 should be applied to the circuit model of the present Application.

Therefore, Applicants submit that the rejection of claims 1 and 8 (as amended) under 35 U.S.C. §101 has been overcome.

Prior Art

In regards to Prior Art, the Office Action stated:

> *Although the claims have been rejected as indefinite and it is unknown where in the disclosure support for the claimed invention exists, the Examiner has cited what appears to be the most relevant prior art.*
> *Although the following is not a rejection under 35 U.S.C. § 102 or 103, Applicants are required by 37 CFR 1.111(c) to point out the patentable distinction of any claimed invention over the prior art references.*
>
> *"Electronic Devices, Second Edition" by Thomas L. Floyd (copyright 1988) discloses a circuit and/or circuit model (Figure 11-5, page 393) comprising a first capacitor connected to the input node and output node ["C"], an input capacitor connected to the input node and to ground ["C(Av+1)"], and an output capacitor connected to the output node and ground ["C((Av+1)/Av)"]. Although Floyd does not explicitly describe "an internal impedance connected to the output node and ground," such a property is inherent to the physical nature of the depicted circuit. The impedance may be infinitely high or infinitely low, nevertheless the impedance is present.*
>
> *"An ideal current source connecting an output node to a voltage*

supply" is an inherent characteristic of a circuit, which by definition generally connects an input and an output to a voltage supply. It is this arrangement that defines the components as a circuit.

Floyd discloses the circuit device described above or its equivalent (Figure 11-7, page 394) further comprising "an output load, having a near capacitor ["C3"], a resistor ["RL"], and a far capacitor ["C2"].

The various functions and output values are inherent in the circuits described by Floyd. Although Floyd does not explicitly describe the functions, they are nevertheless present in the circuits. The functions, which Applicants have not expressly defined in the claims, may be constant functions equal to 0.

Applicants submit that claims 1-10 as amended distinctly claim "a circuit model of a black box circuit stored in the memory" and is accessed by a computer simulation program to simulate the actual response of the black box circuit under any conditions, while hiding the details of the black box circuit from the user (see Lehner , para. 14, 22, 57, 87, 89, Figure 1 ckt A). The circuit model of the claimed invention *uses* models such as miller capacitance, near/far capacitors, resistors, and pi models to derive portions of the black box circuit response during simulation (see Lehner para 12, 24, 51, 65, 87, Fig. 3 and 5-6). For example, a miller capacitance equivalent circuit model may be used to perform one of the capacitance functions recited in claim 1 (see Lehner para. 24, 51 and Fig. 5).

The circuit model of the present invention further differs from conventional textbook models, including the models shown in figures 11-5 and 11-7 of the above cited reference, because it is in an electrical form stored in a memory and accessed by a computer simulation program (see Lehner abstract, summary, para 70, 78, 102 and Fig. 6-8). The circuit model controls portions of the simulation program and causes it to respond to stimuli from a source which is unknown to both the simulation program and the user (see Lehner, para. 22, 80, 87, 89, and 102, and Fig. 7).

Therefore, in accordance with 37 CFR 1.111(c), Applicants submit that the patentable distinction of the claimed invention over the prior art references has been duly noted above, thus *potential* rejection of claims 1 - 10 (as amended) under 35 U.S.C. §102 or §103 has been overcome.

Summary and Conclusion

Based on the foregoing, it is respectfully submitted that the pending claims in the subject patent application are in condition for allowance and that the application may be passed to issuance.

The Examiner is urged to call the undersigned at the number listed below if, in the Examiner's opinion, such a phone conference would aid in furthering the prosecution of this application.

Respectfully submitted,
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Appendix A

Replacement Drawings 1 – 8 (5 sheets)